

FIG. 1 - SYSTEM

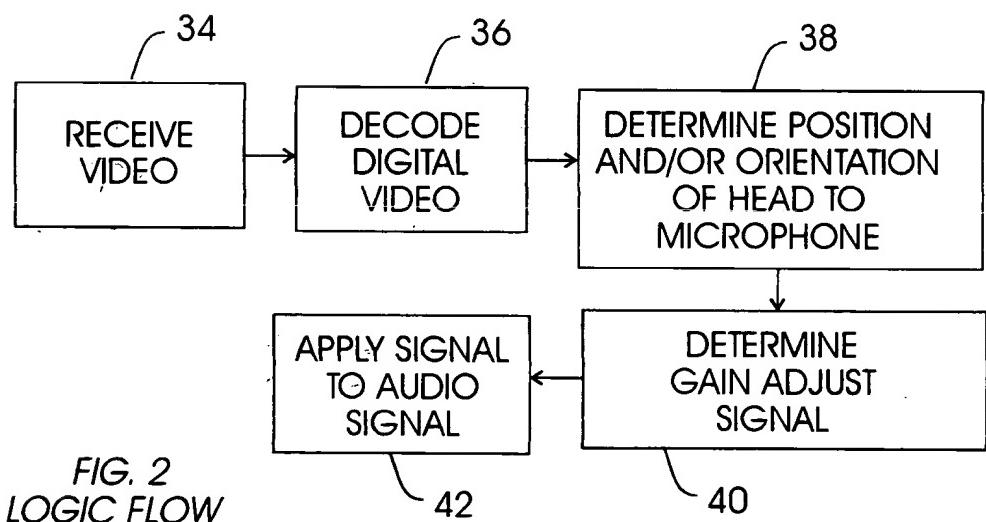


FIG. 2  
LOGIC FLOW

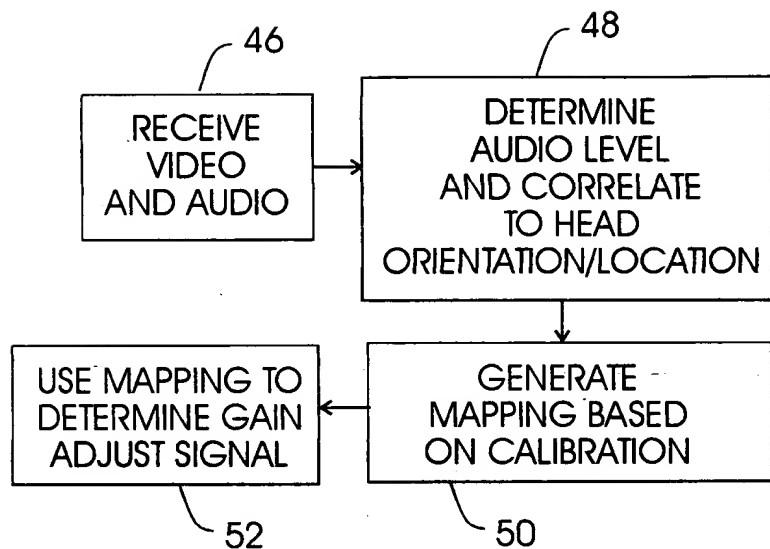


FIG. 3  
LOGIC FLOW FOR AUTOMATIC MAPPING

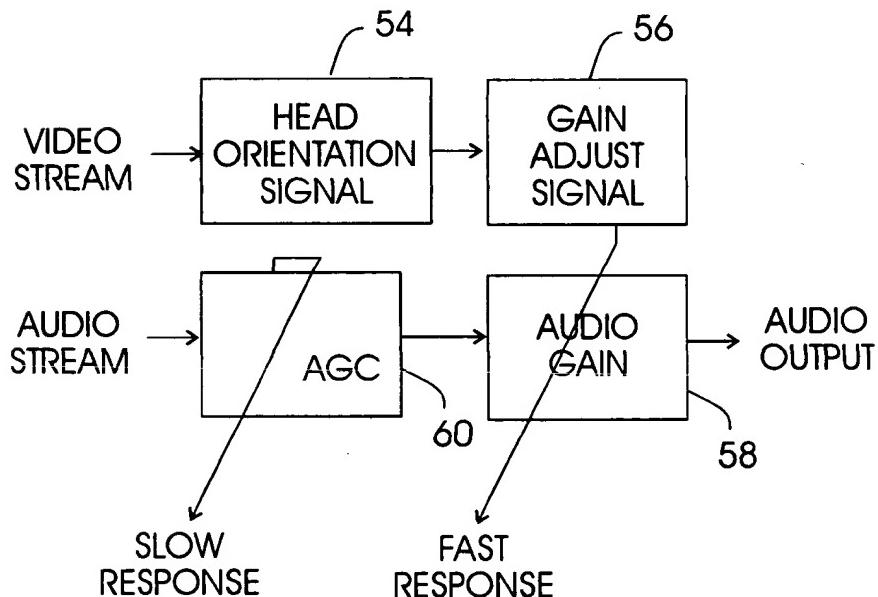


FIG. 4  
DUAL GAIN ADJUST BLOCK DIAGRAM

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